In the Specification:

Please amend paragraphs [0002], [0003], [0012], [0013], [0026]-[0029], and [0034] as noted below.

[0002]Integrated circuits typically operate with power supplies of 5 volts or less and often must drive signals of a particular voltage level on-chip or off-chip. Merely as an example, an integrated circuit pre-amplifier may have a plurality of driver circuits for driving signals off-chip. For instance, an eight bit amplifier for driving eight signals off-chip might have eight driver circuits having an output stage like the output stage ~~100~~ 101 shown in Figure 1 for driving an off-hip load 102 through an output pad 104 of the integrated circuit. Figure 1 shows only the output stage of the driver circuit in detail. The input signal source, V_{IN}, that is to be driven onto the load 102 is supplied to one input terminal of an operational amplifier 105.

[0003]In the output stage ~~100~~ 101, an output transistor M17 has its source coupled to a voltage rail 113, in this case 5 volts, and its drain coupled to node 107. Its gate is coupled to the output of the operational amplifier 105. Transistor M16 has its source coupled to the voltage rail 113, and its drain and gate coupled together to the gate of output transistor M17 and the output of the operational amplifier 105. Transistors M16 and M17 in this circuit are configured as a current mirror that essentially delivers current controlled by the operational amplifier 105 to the load. The input signal VIN is supplied to one input terminal of the operational amplifier and the other input terminal is coupled to the junction 110 of voltage divider 109 comprising resistors R0 and R1. Since an operational amplifier operates to drive the voltages at its two inputs to the same voltage, operational amplifier 105 drives the junction 110 between resistors R0 and R1 to VIN. The voltage at the output pad 104 is dependent on the input voltage, VIN, and the ratio of resistors R0 and R1. Specifically, with this configuration, the output voltage on pad 104 is ((R0 + R1)/R1)*VIN. The current through the load 102 is dictated by the voltage placed on pad 104 and the resistance, R_{ext}, of the load 102. This type of architecture is efficient in that it generates maximum

2

output voltage because the only voltage drop from the rail is the V_{ds} of M17. So the output voltage can go to a maximum value of $VCC - V_{dsM17}$.

[0012]One technique to reduce power dissipation on the chip involves providing a dual power supply comprising a first, higher voltage driver (e.g., 5 volts) and a second, lower voltage driver (e.g., 2.5 volts). When a particular pad (0, 1 …7) is selected, the 5 volt power supply driver is turned on and the 2.5 volt power supply driver is turned off for the selected pad. At the remaining, unselected pads, the 5 volt power supply drivers are turned off and the 2.5 volt power supply drivers are turned on at all unselected pads. This two stage scheme substantially reduces the wasted power dissipation on the chip because a 2.5 volt supply driver instead of 5 volt supply driver can still provide 1 volt across the load, while dumping only 2.5 volts − 1 volt = 1.5 volts per unselected driver, instead of 4 vol<u>t</u>s per unselected driver, inside the chip.

[0013]However, because both the 5 volt power supply driver and the 2.5 volt power supply driver are coupled to the same node, e.g., output pad 104, the output voltage being driven onto the output pad by the 5 volt driver is presented at the output terminal of the 2.5 volt driver. If the 5 volt driver is driving the output pad 104 to a voltage greater than 2.5 + V̶t̶h̶r̶e̶s̶h̶o̶l̶d̶ v̶o̶l̶t̶s̶ <u>the threshold voltage of the transistor in the 2.5 volt power supply that is between the output pad and the 2.5 volt rail</u>, it will cause reverse conduction from the 5 volt rail through output pad 104 to the 2.5 volt rail through the 2.5 volt power supply driver, causing unwanted power dissipation.

[0026]Although the circuit shown in Figures considerably reduces power dissipation on chip relative to the circuit shown in Figure 1, it still suffers from the drawback of reverse conduction. For instance, when the 5 volt driver is selected, depending on V_{IN}, the 5 volt driver stage 201a will drive the output pad to somewhere between 0 and about 4.5 volts. The drain of transistor M7 in the 2.5 volt driver stage 201b is coupled to the output pad 2̶0̶7̶ <u>203</u>. When the 5 volt driver stage 201a is on and the 2.5 volt driver stage 201b is off, transistor M7 will remain off as long as the voltage driven onto the output pad 2̶0̶7̶ <u>203</u> (which is coupled directly to the drain terminal of

3

output transistor M7) remains below about 3.2 volts, i.e., 2.5 volts plus the threshold

voltage (about 0.7 volts) of transistor M7.

[0027]However, when the 5 volt driver stage 201a applies a voltage at the

output pad ~~207~~ 203 greater than 3.2 volts, that voltage on the drain terminal of transistor

M7, ~~which~~ will cause transistor M7 to conduct in the reverse direction as illustrated by

arrow 206. This is a source of unwanted power dissipation in the circuit.

[0028]Figure 4 is a circuit diagram of a modified output stage 400 for a

dual driver circuit in accordance with the present invention. This circuit prevents

reverse conduction in the output stage 401b of the lower voltage (e.g., 2.5 volt) driver

circuit. Relative to the circuit shown in Figures 2 and 3, the following components have

been added. Cascode protection transistor M9 has been added between the drain of

output transistor M7 and the output pad 203. Particularly, the source of cascode

protection transistor M9 is coupled to the drain of output transistor M7 and the drain of

transistor M9 is coupled to the output pad 203. In addition, transistor M10 has been

added as a diode clamp for transistor M9. Its source and gate are tied together and

coupled to the tub of transistor M10. This node is further coupled to the gate of cascode

protection transistor ~~M3~~ M9 and the output of a comparator 405 (described below). Its

drain is coupled to the source of protection transistor M9 at the node between the

source terminal of transistor M9 and the drain terminal of output transistor M7.

Transistor M10 is a diode clamp similar to transistor M5 in the 5 volt driver circuit 201a

and will be explained in further detail below.

[0029] Other changes include that the source of switch transistor M8 has

been uncoupled from the 2.5 volt rail 215 and coupled to a 4 volt rail ~~403~~. Likewise,

logic levels for the select control signal to the gate of transistor M8 and the

demultiplexer are changed to 1 volt to turn the 2.5 volt driver off and 4 volts to turn it on,

instead of 0 and 2.5 volts, respectively. Accordingly, in Figure 4, the SELECT2 control

4

signal of Figures 2 and 3 are replaced with a SELECT3 control signal 408 to reflect the changes in voltage levels. SELECT3 is still the complement of SELECT1.

[0034]As noted above, the bias ~~voltages~~ <u>voltage</u> applied to the source of switch transistor M8 should be 4 volts instead of 2.5 volts (as it was in the prior art circuit of Fig. 2.) Furthermore, the SELECT3 logic levels applied at the gate of switch transistor M8 should be 1 volt to turn the 2.5 volt driver off and 4 volts to turn it on, instead of 0 volts and 2.5 volts, respectively.